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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/669,350	09/26/2000	Kenneth W. Batcher	72255/02661	4571

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EXAMINER
BARQADLE, YASIN M

ART UNIT	PAPER NUMBER
2153	2

DATE MAILED: 06/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/669,350	Applicant(s) BATCHER, KENNETH W.	
	Examiner Yasin M Barqadle	Art Unit 2153	M

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-41 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-41 rejected under 35 U.S.C. 102(e) as being anticipated by Sandorfi US (5768530).

As per claims 1,10, 19, Sandorfi teaches a data processing method and system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

receiving data from a first processing system [Col. 2, lines 60-67 to Col. 3, lines 1-11; abstract];

storing the received data into a first memory device [Fig. 4,52, Col.5, lines 60-67]; and

executing a program instruction on an associated processor

to transfer at least a portion of the stored data to a second memory device[Fig. 4 Col.5, lines 60-67; Col. 9, lines 41-58].

As per claims 2,11 and 20, Sandorfi teaches the invention, wherein the invention further comprises:

transferring at least a portion of the data stored in said second memory device to a third memory device, wherein said second processing system operates upon the data stored in said third memory device [Fig. 15, Col.5, lines 60-67 and Col. 18, lines 51-65].

As per claims 3,12 and 21, Sandorfi teaches the invention, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claims 4,13 and 22, Sandorfi teaches the invention, wherein said third memory device is FIFO memory device [Col.6, lines 47-64].

As per claims 5,12 and 23, Sandorfi teaches the invention, wherein the method further comprises bit-aligning the data in said first memory device [Col.5, lines 34-67].

As per claims 6, 15, 28, and 32, Sandorfi teaches a data transfer method and system for transferring data between two processing systems, wherein said two processing systems operate

independently, said method comprising (Fig. 2):

receiving data from a first processing system [Col. 2, lines 60-67 to Col. 3, lines 1-11; abstract];

storing the received data into a first memory device [Fig. 4,52, Col.5, lines 60-67]; and

transferring the stored data to a second memory device [Col. 4, lines 1-34 and abstract] ; and

executing a program instruction on an associated processor to store at least a portion of the data stored in the second memory device to a third memory device[Fig. 4, Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58].

As per claims 7,16,29 and 33, Sandorfi teaches the invention, wherein said second processing system operates upon the data stored in said third memory device [Fig. 15, Col.5, lines 60-67 and Col. 18, lines 51-65].

As per claims 8,17,30 and 34 Sandorfi teaches the invention, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claims 9,18,31 and 35, Sandorfi teaches the invention, wherein said third memory device is FIFO memory device [Col.6, lines 47-64].

As per claim 24, Sandorfi teaches a system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

a first memory device data received from a first processing system [Fig.4, 52];

a second memory device for receiving data stored in the first memory device [Fig. 1,16]; and

an associated processor for executing a memory read instruction to transfer at least a portion of data stored in the second memory device to a third memory device[Fig. 4, Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58].

As per claim 25, Sandorfi teaches a system according to claim 24, wherein said system comprises a second processing system for operating upon the data stored in said third memory device [Fig. 15, Col.5, lines 60-67 and Col. 18, lines 51-65].

As per claim 26, Sandorfi teaches a system according to claim 24, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claim 27, Sandorfi teaches a system according to claim 24, wherein said third memory device is FIFO memory device [Col.6, lines 47-64].

As per claim 36, Sandorfi teaches a system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

a first memory device for storing data packet received from a first processing system, wherein said data packet includes a header portion and a data portion [Col.5, lines 60-67];

a second memory device for receiving data stored in the first memory device [Fig. 1,16]; and

an associated processor for executing at least one program instruction on to transfer the header portion from the first memory device to a second memory device [Fig. 4, Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58]; and

a hardware logic enabled by the associated processor to transfer the data portion from the first memory device to a third memory device [Fig. 4, Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58].

As per claim 37, Sandorfi teaches a system according to claim 36, wherein said system comprises a second processing system for operating upon the data stored in said third memory device [Fig. 15, Col.5, lines 60-67 and Col. 18, lines 51-65].

As per claim 38, Sandorfi teaches a system according to claim 36, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claim 39, Sandorfi teaches a system according to claim 36, wherein said third memory device is FIFO memory device [Col.6, lines 47-64].

As per claims 40 and 41, Sandorfi teaches a data processing system comprising:

a processor for transferring data to a memory location identified by an address stored in a an address pointer register Fig. 4, Col. 13, lines 8-67 and Col.14, lines 1-55];

a first memory for storing data at a plurality of memory location, each memory location identified by an address register [Fig. 4, Col. 13, lines 8-67 and Col.14, lines 1-55]; and

a FIFO memory for storing data,

wherein the processor receives an instruction to transfer data from a memory location of the first memory identified by the address stored in the address pointer register t the FIFO memory, and automatically increments the address stored in the address having a first parameter identifying the address pointer register, and a second parameter identifying the FIFO memory [Figs 4&5, Col.5, lines 60-67; Col. 13, lines 8-67 and Col.14, lines 1-55; Col.19, lines 19-63].

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yasin M Barqadle whose telephone number is 703-305-5971. The examiner can normally be reached on 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-304-3900.

Yasin Barqadle

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